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| EXAMINER | |
|---|---|
| AGGARWAL, YOGESH K | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2622 | |

DATE MAILED: 08/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/829,114 | KIMURA, HAJIME | |
| | Examiner | Art Unit | |
| | Yogesh K. Aggarwal | 2622 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *05 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,2,35,36,41,57,58 and 89-106* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,35,36,41,57,58 and 89-106* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

***Response to Arguments***

1. Applicant's arguments filed 06/05/2006 have been fully considered but they are not persuasive.

**Examiner's response:**

2. Applicant argues with regards to claim 1 that Clark does not teach "wherein an absolute value of a voltage between a gate and a source of the biasing transistor is higher than an absolute value of a threshold voltage of the biasing transistor". The Examiner respectfully disagrees. Clark teaches transistor 214 is controllably biased to have a higher drive in order to pre-discharge capacitor 212 and a pre-discharge is formed by modulating the gate voltage of the transistor (col. 5 lines 11-20) i.e. during at least a pre-discharge period of the capacitor, a pre-discharge current flows through transistor 214. A threshold voltage is defined in IEEE dictionary as minimum gate voltage necessary for onset of current flow between source and drain of a transistor. Therefore it is noted that in order for the current to flow during a pre-discharge period through transistor 214, a modulating gate to source (VSS is ground, See figure 2) higher than a threshold voltage has to be applied. Hence Clark meets the claimed limitations. As specified in applicant's specification on page 36 lines 6-10, "... **other than during the pre-discharge period,** an optimum value of an absolute value of a bias signal electric potential (voltage between the gate and the source of the biasing transistor) is an electric potential that is slightly higher than an absolute value of a threshold voltage of the biasing transistor 1102" is not claimed.

3. Applicant argues with regards to claim 3 (now cancelled) that Clark fails to teach electric discharging power source line connected to the biasing power source line. Clark teaches that the

electric discharging transistor 216 power source line and the biasing transistor 214 power source line is connected to ground (See figure 2). Therefore both are connected via ground. As explained in Applicant's specification on Page 38 lines 19-23 "Normally, the electric potential of the electric discharging power source line 1109 may be set equivalent to that of the biasing side power source line 1104. Therefore the electric discharging power source line 1109 and the biasing side power source line 1104 may be connected."

4. Applicant arguments regarding claim 58 do not overcome 35 USC 112 rejections. As Specified in Applicant's specification at page 37 line 20-page 38 line 18 discloses it is necessary that the electric potential of the electric discharging power source line 1109 be set higher than the electric potential of the biasing side power source line 1104 but lower than the electric potential of the bias signal line 1106 **during the pre-discharge period** is not claimed.

***Claim Rejections - 35 USC § 112***

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claim 58 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The claim recites "wherein a value of an electric potential of the electric discharging power source line takes a value that is between an electric potential of the bias signal line and an electric potential of the biasing side power source line". According to the specification electric discharging power source line 1109 (figure

11a) and biasing side power source line 1104 are grounded. The bias signal line 1106 is shown at a voltage Vb (figure 11b). Therefore the value of value of an electric potential of the electric discharging power source line (ground voltage) is not between a potential of the bias signal line (Vb) and potential of the biasing side power source line (Ground). Therefore as explained above, a pre-discharge period during which the a value of an electric potential of the electric discharging power source line takes a value that is between an electric potential of the bias signal line and an electric potential of the biasing side power source line is not claimed.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 2, 8, 9, 35, 36, 41, 57, 89-92 and 98-101 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Clark (US Patent # 6,157,016). [Claims 1, 89, 98]

Applicant's admitted prior art teaches a semiconductor device (figure 8) comprising an amplifying transistor (801), a biasing transistor (802), an amplifying side power source line (803); a biasing side power source line (804); a bias signal line (802). Applicant's admitted prior art discloses in figure 8 a drain terminal of the amplifying transistor being connected to the amplifying side power source line (803), a source terminal of the biasing transistor is connected to the biasing side power source line (804), a source terminal of the amplifying transistor (801) is connected to a drain terminal of the biasing transistor, a gate terminal ($V_b$) of the biasing

transistor (802) is connected to the bias signal line, a gate terminal of the amplifying transistor (801) serves as an input terminal ($V_{in}$), and a source terminal of the amplifying transistor (801) serves as an output terminal ($V_{out}$, Paragraphs 24 and 25). Applicant's prior art (figure 8a) teaches power source standard line 804 connected to ground.

Applicant's admitted prior art fails to teach an electric discharging transistor and an electric discharging power source line connected to the biasing side power source line wherein one of the output terminal and the electric discharging power source line is connected to a source terminal of the electric discharging transistor while the other thereof is connected to a drain terminal of the electric discharging transistor, and on an absolute value of a voltage between a gate and a source of the biasing transistor is equivalent to a minimum value of an absolute value of a voltage between a gate and a source that is necessary for making the biasing transistor into a conductive state.

However Clark et al. teaches a first circuit comprising source follower circuit made up of a source follower device 204 and a load device 214 and the pixel access device 208 (col. 3 line 66-col. 4 line 21, figure 2). An electric discharging transistor 216 source's terminal (used to predischarge bitline capacitor 212) is coupled to the source of the pixel access transistor 208 (that is part of the source follower circuit used as an amplifier, col. 4 lines 21-55). Clark teaches that the electric discharging transistor 216 power source line and the biasing transistor 214 power source line is connected to ground (See figure 2). Therefore both are connected via ground. Clark further teaches that transistor 214 may be controllably biased to have a higher drive by modulating the gate voltage of transistor 214, with high voltage for discharge (col. 5 lines 11-20) i.e. during at least a pre-discharge period of the capacitor, a pre-discharge current flows through

transistor 214. A threshold voltage is defined in IEEE dictionary as minimum gate voltage necessary for onset of current flow between source and drain of a transistor. Therefore it is noted that in order for the current to flow during a pre-discharge period through transistor 214, a modulating gate to source (VSS is ground, See figure 2) higher than a threshold voltage has to be applied.

Therefore taking the combined teachings of Applicant's admitted prior art and Clark, it would have been obvious to one skilled in the art at the time of the invention to have been motivated to have an electric discharging transistor and an electric discharging power source line connected to the biasing side power source line wherein one of the output terminal and the electric discharging power source line is connected to a source terminal of the electric discharging transistor while the other thereof is connected to a drain terminal of the electric discharging transistor on an absolute value of a voltage between a gate and a source of the biasing transistor is equivalent to a minimum value of an absolute value of a voltage between a gate and a source that is necessary for making the biasing transistor into a conductive state in order to cause reduction of the time delay otherwise imposed if the pixel was first selected for readout and therefore increases the speed of the pixel as taught in Clark (col. 3 lines 1-5). [Claims 2, 90, 99]

Applicant's admitted prior art teaches a load capacitance (805) wherein one terminal of the load capacitance is connected to the output terminal ($V_{out}$), and the other terminal of the load capacitance is connected to a load capacitance power source line (806).

[Claims 8, 91, 100]

Applicant's admitted prior art teaches an area sensor having plurality of pixels with one biasing transistor for one output line (Paragraph 11, figure 3, output line 303). Therefore for a plurality of output lines corresponding to plurality of pixels there will be plurality of biasing transistors. Clark further teaches that transistor 214 may be controllably biased to have a higher drive by modulating the gate voltage of transistor 214, with high voltage for discharge (col. 5 lines 11-20).

[Claims 9, 92, 101]

Clark teaches that the amplifying transistor, the biasing transistor, and the electric discharging transistor are transistors having the same polarity (NMOS, col. 3 line 65-col. 4 line 55, figure 2).

[Claims 35 and 57]

These are method claims corresponding to apparatus claim 1 except "wherein the discharging transistor will be used to perform a discharge when the discharging transistor is in a conductive state". Clark teaches that the discharging transistor 216 is biased to be in full conduction before pixel 218 is read out, thereby predischarging capacitor 212 to approximately 0 volts (col. 4 lines 41-45).

[Claim 36]

This is a method claim corresponding to apparatus claim 2. Therefore it has been analyzed and rejected based upon apparatus claim 2.

[Claim 41]

This is a method claim corresponding to apparatus claim 8. Therefore it has been analyzed and rejected based upon apparatus claim 8.

9. Claims 10-14, 93-97 and 102-106 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art, Clark et al. (US Patent # 6,157,016) and in further view of Silver et al. (US Patent # 6,690,842).

[Claims 10-14]

Applicant's admitted prior art in view of Clark teaches the limitations of claim 1. Clark et al. teaches that the semiconductor device can be used in a camera or any imaging devices (Also read as a computer or portable communication terminal, col. 3 lines 15-20) but fails to teach other devices like X-ray and a scanner. However Silver et al. teaches that for forming digital images a number of devices like a digital camera, line-scan scanners, X-ray devices such as CT scanners can be used (col. 1 lines 15-20). Therefore taking the combined teachings of Applicant's admitted prior art, Clark et al. and Silver, it would have been obvious to one skilled in the art at the time of the invention to have been motivated to use the semiconductor device of Clark into other devices like X-ray and a scanner. The benefit of doing so would be a reduction in cost of manufacture because the same imaging sensor might be used in a number of devices.

***Conclusion***

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K. Aggarwal whose telephone number is (571) 272-7360. The examiner can normally be reached on M-F 9:00AM-5:30PM.

11. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivek Srivastava can be reached on (571)-272-7304. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

YKA
July 30, 2006

VIVEK SRIVASTAVA
PRIMARY EXAMINER